IN THE CLAIMS:

1. (Currently Amended) A transistor, comprising:

a substrate;

an active region defined in said substrate;

a gate insulation layer formed above said active region; ~~and~~

a gate electrode formed above said gate insulation layer, said gate electrode having a middle portion located over the active region, said middle portion having an extension of an upper part along the gate length direction that decreases from bottom to top of the upper part, and said middle portion also having a gate length and a gate height, wherein a cross-sectional area of said gate electrode in a plane defined by said gate length and said gate height of the middle portion exceeds a value obtained by multiplying the gate length by the gate height; and

a metal silicide layer formed on at least a portion of said gate electrode.

2. (Previously Presented) The transistor of claim 1, wherein a lower part of said middle portion has a cross-sectional area in the plane defined by the gate length and the gate height that is substantially rectangular.

3. (Canceled)

4. (Previously Presented) The transistor of claim 1, wherein the gate length is 100 nm or less.

5. (Previously Presented) The transistor of claim 1, wherein sidewalls of the lower part are, at least partially, covered by thermally grown silicon dioxide.

6. (Previously Presented) The transistor of claim 1, wherein the gate electrode comprises polycrystalline silicon and a metal.

7. (Previously Presented) The transistor of claim 1, wherein the upper part comprises a metal.

8. (Previously Presented) The transistor of claim 1, wherein the substrate is a semiconductor substrate.

9. (Previously Presented) The transistor of claim 1, wherein the substrate is an insulating substrate, and the active region is formed in a semiconductor layer deposited over the insulating substrate.

10. (Withdrawn) A method of manufacturing a field effect transistor having an improved signal performance, the method comprising:

providing a substrate and defining an active region therein;

forming a gate insulation layer over the active region;

depositing a first gate electrode material layer having a first thickness and patterning a first portion of a gate electrode, the first portion having a height substantially equal to the first thickness;

depositing an insulating layer having a thickness determined by the first thickness;

planarizing the insulating layer to expose a surface of the first portion;

selectively removing material of the planarized insulating layer so as to reduce the thickness of the insulating layer until a predefined adjustment thickness is obtained to partially expose sidewalls of the first portion;

depositing a second gate electrode material layer over the insulating layer and the first portion; and

anisotropically etching the second gate electrode material layer to form a gate electrode including the first portion and an extension portion laterally extending beyond the first portion, wherein a cross-sectional shape of the extension portion is determined by the adjustment thickness.

11. (Withdrawn) The method of claim 10, wherein the first gate electrode material layer and the second gate material layer comprise polycrystalline silicon.

12. (Withdrawn) The method of claim 11, further comprising depositing a metal layer over the gate electrode and initiate a chemical reaction of the metal layer and the polycrystalline silicon.

13. (Withdrawn) The method of claim 10, wherein the first thickness is in the range from 1-2.5 μm.

14. (Withdrawn) The method of claim 10, wherein the insulating layer comprises at least one of silicon dioxide and silicon nitride.

15. (Withdrawn) The method of claim 10, wherein selectively removing material of the insulating layer comprises using a slow chemical etch solution that is highly selective with respect to the first gate electrode material layer.

16. (Withdrawn) The method of claim 10, wherein selectively removing material of the insulating layer comprises forming one or more etch stop layers on the first portion prior to depositing the insulating layer.

17. (Withdrawn) The method of claim 16, wherein at least one of the one or more etch stop layers comprises thermally grown silicon dioxide, wherein a thickness of the thermally grown silicon dioxide affects the shape of the extension portion.

18. (Withdrawn) The method of claim 17, further comprising removing the one or more etch stop layers prior to depositing the second gate electrode material layer.

19. (Withdrawn) The method of claim 17, wherein the insulating layer comprises silicon nitride.

20. (Withdrawn) The method of claim 16, wherein at least one of the one or more etch stop layers is formed by ion implantation.

21. (Withdrawn) The method of claim 10, wherein depositing the second gate electrode material layer comprises depositing two or more layers.

22. (Withdrawn) The method of claim 21, wherein the two or more gate electrode material layers comprise different materials.

23. (Withdrawn) The method of claim 22, wherein one of the two or more gate electrode material layers comprises a metal.

24. (Withdrawn) The method of claim 10, wherein the substrate is a semiconductor substrate.

25. (Withdrawn) The method of claim 10, wherein the substrate is an insulating substrate and the method further comprises forming a layer of active material over the insulating substrate.

26. (Withdrawn) The method of claim 10, wherein the extension portion is used as an implantation mask during formation of the drain and source.

27. (Currently Amended) A transistor, comprising:

a substrate;

a gate insulation layer formed above said substrate; ~~and~~

a gate electrode formed above said gate insulation layer, said gate electrode having an upper portion comprised of polysilicon and a lower portion, said upper portion having a plurality of metal extensions formed on said upper portion comprised of polysilicon, said metal extensions of said upper portion comprised of polysilicon extending laterally beyond said lower portion of said gate electrode by an amount that decreases from bottom to top of the upper portion; and

a metal silicide layer formed on at least a portion of said gate electrode.

28. (Previously Presented) The transistor of claim 27, further comprising an insulating material positioned adjacent said lower portion of said gate electrode and under said extensions formed on said upper portion.

29. (Previously Presented) The transistor of claim 27, wherein said substrate is comprised of silicon.

30. (Previously Presented) The transistor of claim 27, wherein said gate insulation layer is comprised of silicon dioxide.

31. (Previously Presented) The transistor of claim 27, wherein said lower portion of said gate electrode is comprised of polysilicon.

32. (Canceled)

33. (Previously Presented) The transistor of claim 27, wherein said extensions are comprised of polysilicon.

34. (Previously Presented) The transistor of claim 27, wherein said upper portion of said gate electrode and said extensions have a combined lateral dimension that is approximately 5-100 percent greater than a lateral dimension of said lower portion of said gate electrode.

35. (Currently Amended) A transistor, comprising:

a substrate;

a gate insulation layer formed above said substrate;

a gate electrode formed above said gate insulation layer, said gate electrode comprised of

a plurality of sidewalls, said gate electrode having an upper portion comprised of polysilicon and a lower portion, said upper portion having a plurality of extensions formed thereon, said extensions of said upper portion extending laterally beyond said lower portion of said gate electrode by an amount that decreases from bottom to top of the upper portion; ~~and~~

an etch stop layer covering at least a portion of said sidewalls of said gate electrode; and

a metal silicide layer formed on at least a portion of said gate electrode.

36. (Previously Presented) The transistor of claim 35, further comprising an insulating material positioned adjacent said lower portion of said gate electrode and under said extensions formed on said upper portion.

37. (Previously Presented) The transistor of claim 35, wherein said substrate is comprised of silicon.

38. (Previously Presented) The transistor of claim 35, wherein said gate insulation layer is comprised of silicon dioxide.

39. (Previously Presented) The transistor of claim 35, wherein said lower portion of said gate electrode is comprised of polysilicon.

40. (Previously Presented) The transistor of claim 35, wherein said extensions are comprised of polysilicon.

41. (Previously Presented) The transistor of claim 35, wherein said upper portion of said gate electrode and said extensions have a combined lateral dimension that is approximately 5-100 percent greater than a lateral dimension of said lower portion of said gate electrode.

42. (Previously Presented) The transistor of claim 35, wherein said etch stop layer is comprised of a thermally grown layer of silicon dioxide.